EUROPEAN PATENT APPLICATION

(12)

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(54) Data delay/memory circuit.

(57) A data delay/memory circuit includes clock-controlled data latch circuits formed with cascade-connected clocked inverters (I1-I7). The data delay/memory circuit also includes a clock generator (CG) for supplying the clocked inverters (I1-I7) with clock signals ($\phi1$-$\phi7$, $\overline{\phi1}$-$\overline{\phi7}$). These clock signals ($\phi1$-$\phi7$, $\overline{\phi1}$-$\overline{\phi7}$) have individual clocking phases and are sequentially generated such that the clocking phase for a final stage (I7) of the data latch circuits is ahead of that for an initial stage (I1) thereof.
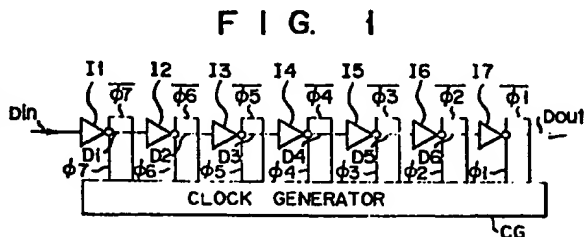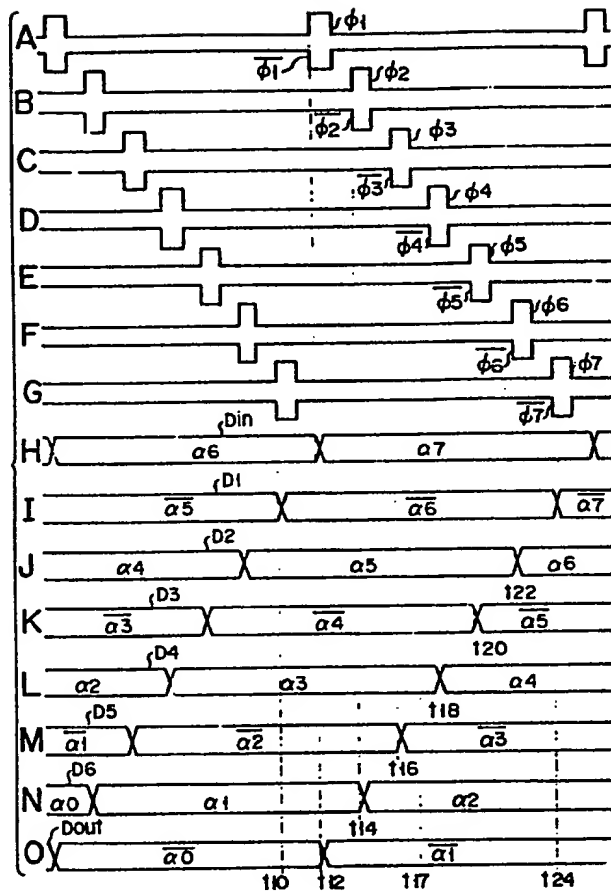
F I G. 1

CLOCK GENERATOR

EP 0 171 720 A2

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FIG. 2

- 1 -

Data delay/memory circuit

The present invention relates to a data
delay/memory circuit which memorizes input data
for a given period of time and, thereafter, outputs
the memorized data.

5   Signal processing for temporary memorizing and
delaying a digital signal is conventionally effected in
a digital 1H memory which delays by one horizontal
period of time (1H) a horizontal video signal of a
digital TV, in a digital filter, in a deinterleave

10   circuit of a compact disc player, or in the like.
In a prior art data delay/memory circuit used for
the above exemplified applications, a plurality of
cascade-connected one-bit shift registers are conven-
tionally adapted. The number of the cascade connections

15   depends on the circuit design. Each of these one-bit
shift registers comprises a pair of clocked inverters
for latching input data. One clocked inverter of the
pair operates in synchronism with a clock signal, while
the other clocked inverter operates in synchronism with

20   an antiphase clock signal. According to such a prior
art data delay/memory circuit, a one shift register is
inevitably provided for storing each one bit data.
Consequently, the necessary number of the data latching,
clocked inverters has to be twice the number of the one

25   bit shift registers. If a 1H memory of a digital TV

which requires a large memory capacity of, e.g., 1135
bits is constituted by such a data delay/memory circuit,
the number of circuit elements becomes numerous. For
this reason, when such a data delay/memory circuit

5   is circuit-integrated, a prominently large chip size
is required, resulting in a decrease of the yield of IC
manufacture while increasing the cost thereof.

It is, accordingly, an object of the present
invention to provide a data delay/memory circuit which

10   allows for a decrease in the necessary number of circuit
elements for one bit, thereby reducing the size of the
IC chip and improving the yield of IC manufacture.

To achieve the above object, the present invention
employs a data shift circuit formed with a plurality of

15   multiply or serially cascade-connected data latch
circuits, the plural data latch circuits being con-
trolled by different clock signals. These clock signals
have individual clocking phases and are sequentially
generated in such a manner that the clocking phase for a

20   final stage of the data latch circuits is ahead of that
for an initial stage thereof. According to the present
invention, (N + 1) data latch circuits satisfactorily
constitute an N bit data delay/memory circuit.

According to the present invention, the necessary

25   number of circuit elements per one bit can be effec-
tively decreased, thereby reducing the chip size of the
IC and lowering the manufacturing cost.

This invention can be more fully understood from
the following detailed description when taken in

30   conjunction with the accompanying drawings, in which:

Fig. 1 shows a basic configuration of a data
delay/memory circuit according to an embodiment of the
present invention;

Figs. 2A to 2O show a timing chart explaining the

35   circuit operation of Fig. 1;

Fig. 3 shows a circuit configuration of one
application of the Fig. 1 circuit;

Figs. 4A to 4V show a timing chart explaining the circuit operation of Fig. 3;

Fig. 5 shows an arrangement of the wiring for feeding clock signals applied to the circuit of Fig. 3;

Fig. 6 shows a digital low-pass filter utilizing the circuit of Fig. 3;

Fig. 7 shows a digital high-pass filter utilizing the circuit of Fig. 3;

Fig. 8 shows a deinterleave circuit for a CD (compact disc) to which the circuit of Fig. 3 is applied;

Fig. 9 is a timing chart partially showing the relation between input data and output data; and

Figs. 10A to 10E respectively show modifications of each of the latch circuits (I1 to I7) in Fig. 1.

In the following, preferred embodiments of this invention will be described with reference to the accompanying drawings.

Fig. 1 shows a circuit configuration of a data delay/memory circuit according to one embodiment of the present invention. This circuit is designed to memorize and to delay 6-bit data. In the figure, seven clocked inverters I1 to I7 are multiply or serially cascade-connected. Each of these clocked inverters may be made of a CMOS circuit formed with P-channel and N-channel MOS transistors. The gates of the N-channel MOS transistors receive clock signals $\phi 1$ to $\phi 7$. The gates of the P-channel MOS transistors receive clock signals $\overline{\phi 1}$ to $\overline{\phi 7}$, which are antiphased to clock signals $\phi 1$ to $\phi 7$, respectively. Clock signals $\phi 1$ to $\phi 7$ and $\overline{\phi 1}$ to $\overline{\phi 7}$ are obtained from a clock generator CG. (The generation timing of these clock signals $\phi 1$ to $\phi 7$ and $\overline{\phi 1}$ to $\overline{\phi 7}$ are shown in Figs. 2A to 2G.)

Input data Din is supplied to the initial stage clocked inverter I1 and, after a certain time delay, the final stage clocked inverter I7 delivers output data Dout corresponding to the input data Din.

As seen from the timing chart of Figs. 2A to 2G, and from the circuit configuration of Fig. 1, the individual phase delays of clock signals $\phi 1$ to $\phi 7$ (or $\overline{\phi 1}$ to $\overline{\phi 7}$) are gradually increased from the final stage side (I7) toward the initial stage side (I1).

The above clocked inverters I1 to I7, which are controlled by clock signals $\phi 1$ to $\phi 7$ and by antiphase clock signals $\overline{\phi 1}$ to $\overline{\phi 7}$, constitute a dynamic data latch circuit.

Figs. 2A to 2$\underline{0}$ show a timing chart illustrating the clock signals as well as the contents of data latched in the clocked inverters of Fig. 1. The circuit operation of the Fig. 1 embodiment will be described below with reference to this timing chart.

Assume that, immediately after the generation of clock signal $\phi 7$, which is supplied to initial stage clocked inverter I1 at time t10, the contents of data D1, output from initial stage clocked inverter I1 becomes $\overline{\alpha 6}$ (after t10 in Fig. 2I). Also assume that output data D2 to D7, from the following clocked inverters I2 to I7, are $\alpha 5$, $\overline{\alpha 4}$, $\alpha 3$, $\overline{\alpha 2}$, $\alpha 1$ and $\overline{\alpha 0}$, respectively, at time t10 (Figs. 2J-2$\underline{0}$).

According to the Fig. 1 circuit, initial clock signal $\phi 1$, to be generated first, is supplied to clocked inverter I7 which constitutes the final stage of the cascade-connected seven clocked inverters I1 to I7. When clock signal $\phi 1$ is generated under the above assumption (t12 in Fig. 2A), final stage clocked inverter I7 inverts the phase of data D6, output from preceding clocked inverter I6 (from $\alpha 1$ to $\overline{\alpha 1}$ in Figs. 2N and 2$\underline{0}$). Thus, after the generation of clock signal $\phi 1$, the contents of output data Dout from final stage clocked inverter I7 are changed from $\overline{\alpha 0}$ to $\overline{\alpha 1}$ (after t12 in Fig. 2$\underline{0}$). Further, when the subsequent clock signal $\phi 2$ is generated (t12 in Fig. 2B), clocked inverter I6 is operated so that the phase of data D5, output from clocked inverter I5, is inverted. After generation of

clock signal $\phi 2$, the contents of data D6, output from clocked inverter I6, are changed from $\alpha 1$ to $\alpha 2$ (after t14 in Fig. 2N).

Similarly, clocked inverters I5 to I2 are sequentially operated by the subsequent generation of clock signals $\phi 3$ to $\phi 6$ (Figs. 2C to 2F), so that the respective outputs from the preceding stages are sequentially phase-inverted. After completion of the generation of these clock signals, the contents of output data D5 to D2 from clocked inverters I5 to I2 are set at $\overline{\alpha 3}$ (after t16 in Fig. 2M), $\alpha 4$ (after t18 in Fig. 2L), $\overline{\alpha 5}$ (after t20 in Fig. 2K) and $\alpha 6$ (after t22 in Fig. 2J), respectively.

When clock signal $\phi 7$ is generated (t24 in Fig. 2G), the initial stage clocked inverter I1 is operated so that the phase of input data Din is inverted (from $\alpha 7$ to $\overline{\alpha 7}$ in Figs. 2H and 2I). After the generation of clock signal $\phi 7$, the contents of output data D1, from initial stage clocked inverter I1, are changed from $\overline{\overline{\alpha 6}}$ to $\overline{\overline{\alpha 7}}$ (after t24 in Fig. 2I).

During the period from time t10 to t24, seven clocked inverters I1 to I7 store at least 6 bits of data. The minimum bit number 6 of the stored data is obtained when the same data is stored in two clocked inverters. For instance, at time t17, clocked inverter I4 stores data $\alpha 3$ (Fig. 2L) which is substantially the same as the data $\overline{\alpha 3}$ (Fig. 2M) stored in clocked inverter I5, except for its phase.

According to the circuit configuration of the above embodiment, storing and delaying of 6 bits of data can be achieved only by seven clocked inverters. When the number of the circuit elements of the present invention is compared with that of the said prior art circuit, five clocked inverters can be saved according to the present invention.

Generally speaking, according to the present invention, (N + 1) clocked inverters are satisfactory to

achieve the storing and delaying of N bits data. From
this, the number of elements required for the circuit
integration is considerably reduced when the bit number
of the circuit is large. Accordingly, the IC chip size
5   and IC manufacturing cost can also be effectively
reduced.

In the above embodiment, many data transferring
clock signals $\phi 1$ to $\phi 7$ are employed. These clock
signals may be simply obtained by frequency-dividing
10   a master (or system) clock signal delivered from an
oscillator. In this case, the period of these
transferring clock signals $\phi 1$ to $\phi 7$ is longer than that
of the master clock signal, and the required data
transfer rate can be lowered beyond that required when
15   the data transfer is carried out with the master clock
signal in conjunction with its phase-inverted signal,
this being one of the advantages obtained by the
configuration of Fig. 1.

Fig. 3 shows a circuit configuration of a typical
20   application of the present invention. According to this
circuit application, a high data transferring rate based
on master clocks ($\phi s1$, $\phi s2$) can be obtained while enjoy-
ing the advantage (reduction in the required number of
the circuit elements) of this invention.

25   According to a data delay/memory circuit of this
application, six data delay/memory circuits, DMC1 to
DMC6, each of which may have the same configuration as
Fig. 1, are parallel arranged, thereby achieving 6 bits
data storing and delaying.

30   The data input side of DMC1 to DMC6 is coupled to a
data serial/parallel converter circuit SPC. Converter
SPC includes 6 sets of cascade-connected data delay
circuits DL10 to DL20. Circuits DL10 to DL20 are re-
spectively formed with CMOS clocked inverter pairs I10
35   to I21, each pair of which is controlled by dual-phase
master clock signals $\phi s1$ and $\phi s2$. The data output sides
of DMC1 to DMC6 are coupled to a data parallel/serial

converter circuit PSC. Converter PSC includes 6 sets of
cascade-connected data delay circuits DL22 to DL32.
Circuits DL22 to DL32 are respectively formed with CMOS
clocked inverter pairs I22 to I33, each pair of which is
controlled by dual-phase master clock signals $\phi s1$ and
$\phi s2$. Respective outputs Din1 to Din6, from data delay
circuits DL10 to DL20, in SPC are supplied to DMC1 to
DMC6. Respective delayed output data Dout1 to Dout6,
from DMC1 to DMC6, are supplied to the corresponding
data delay circuits DL22 to DL32 in PSC.

The above converter circuit SPC distributes to DMC1
to DMC6 the serial data (numbered by 0-41) supplied to
the initial stage (DL10) of data delay circuits, in
accordance with the dual-phase master clock signals $\phi s1$
and $\phi s2$. Conversely, converter circuit PSC progres-
sively delays output data Dout1 to Dout6 for each one
bit of the data delay circuits in synchronism with the
dual-phase master clock signals $\phi s1$ and $\phi s2$, so that the
delayed parallel data Dout1 to Dout6 are sequentially
converted into serial data, and transferred to the
circuit end (I33) of PSC. Data Dout1 to Dout6 are
obtained by the distributing operation of SPC, and are
stored and delayed in parallel by DMC1 to DMC6.

Figs. 4A to 4V show a timing chart explaining the
circuit operation of Fig. 3.

Assume a case wherein 41st to 36th data, as shown at
time t40 in Figs. 4J to 4$\underline{0}$, are supplied to DMC1 to DMC6
as input data Din1 to Din6. Assume further that DMC1 to
DMC6 respectively store individual data numbered as shown
in Fig. 3. In this case, the respective contents of
parallel output data Dout1 to Dout6, from DMC1 to DMC6,
become 5th to 0th data as shown in Figs. 4P to 4V.

Output data Dout1 to Dout6, from DMC1 to DMC6, are
sequentially transferred via respective data delay
circuits DL22 to DL32, operated in synchronism with
master clock signals $\phi s1$ and $\phi s2$. Then, final output
data DY which is synchronized with master clock signals

φsl and φs2 is delivered from the circuit end of PSC.
Thus, the rate of data transfer can be made substan-
tially the same as the master clocking rate, according
to the circuit configuration of Fig. 3. In addition,

5   according to this circuit arrangement, only 66 circuit
elements (42 elements for DMC1 to DMC6, 12 elements
for SPC, and 12 elements for PSC) are necessary to
constitute a 36 bits data delay/memory circuit (which
is formed with 6 bits × 6 DMC blocks). In contrast,

10   according to a prior art circuit depending on master
clock signals alone, 72 circuit elements (= 36 bits × 2)
are required. Thus, 6 circuit elements can be saved
according this embodiment, the number of saved circuit
elements being much increased as the number of bits

15   becomes large.

Fig. 5 shows a wiring arrangement for clock signals
when DMC1 to DMC6 in the embodiment of Fig. 3 are
arranged in parallel in the IC. As may be seen from
Fig. 5, wirings W10 to W23, for feeding respective clock

20   signals (φ1-φ7 & $\overline{φ1}$-$\overline{φ7}$), are arranged perpendicular to
the data transferring direction (horizontal in the
figure) of seven cascade-connected clocked inverters I1A
to I7A. When such a wiring arrangement is employed, the
total area of the wiring pattern is smaller than that

25   where respective data delay/memory circuits utilize
individual wirings which are parallel along the data
transferring direction of clocked inverters I1A to I7A.

Fig. 6 shows a digital low-pass filter utilizing
the circuit of Fig. 3. A digital input signal DX is

30   supplied to a data delay/memory circuit 100 which may
have the circuit configuration of Fig. 3. Input signal
DX may be obtained by A/D converting an analog voice
signal, video signal or the like. A digital output
signal DY is supplied to an adder 60. Input signal DX

35   is added to output signal DY in adder 60. An output
signal DZ from adder 60 has an amplitude component
double that of input signal DX. Prescribed high

frequency components of signal DZ are filtered off by
the circuit operation of Fig. 6.

Fig. 7 shows a digital high-pass filter utilizing
the circuit of Fig. 3. Digital input signal DX is
supplied to data delay/memory circuit 100 having the
circuit configuration of Fig. 3. Input signal DX may be
obtained by A/D converting an analog video signal or the
like. When input signal DX is a video signal, the delay
time of the Fig. 3 circuit is selected to be one hori-
zontal scanning period (1H) of a TV system. Digital
output signal DY is supplied to the negative input of a
subtracter 70. Input signal DX is supplied to the
positive input of subtracter 70. Output signal DZ from
subtracter 70 corresponds to DX - DY. Prescribed low
frequency components of signal DZ are filtered off by
the circuit operation of Fig. 7.

Fig. 8 shows a deinterleave circuit for a CD
(compact disc) to which the circuit of Fig. 3 is
applied. Fig. 9 is a timing chart showing the relation
between input data IN and output data OUT of the Fig. 8
circuit. In this deinterleave circuit, a delay time D
is assumed to be 4T, where T denotes a period of each of
the data of the CD. Since D = 4T, five clock signals $\phi 0$
to $\phi 4$ are provided. Each of these clock signals $\phi 0$ to
$\phi 4$ has an individual phase, as in the case of the Fig. 3
embodiment (cf. Figs. 4C-4G), and is supplied to data
delay/memory circuits DMC1 to DMC27. According to the
circuit operation of Fig. 8, interleaved data IN is
deinterleaved as shown in Fig. 9.

Figs. 10A to 10E, respectively, show modifications
of each of latch circuits I1 to I7 in Fig. 1. The latch
circuits of Fig. 1 are dynamic clocked inverters. In
contrast, the latch circuit of Fig. 10A is a static
latch formed of a clocked inverter. The latch circuit
of Fig. 10B is a dynamic latch formed of a transmission
gate being formed with P and N channel MOS transistors.
The latch circuit of Fig. 10C is a dynamic latch formed

of a transmission gate being formed with an N channel
MOS transistor. The latch circuit of Fig. 10D is a
static latch formed of a transmission gate being formed
with P and N channel MOS transistors. The latch circuit
5   of Fig. 10E shows another static latch formed of a
clocked inverter.

The present invention should not be limited to the
above-mentioned embodiments, various modifications can
be made thereof. Although the circuit of Fig. 3 employs
10 six data delay/memory circuits DMC1 to DMC6 arranged in
parallel with each storing and delaying 6 bits of data,
the number of bits of each DMC1 to DMC6 may differ from
the number of the parallel arranged data delay/memory
circuits. For instance, twelve data delay/memory cir-
15 cuits, each of which stores and delays 6 bits of data,
may be parallel arranged. In this case, the period of
clock signals used for controlling the clocked inverters
of the respective data delay/memory circuits becomes
double the period needed when six data delay/memory
20 circuits are parallel arranged, thereby increasing the
margin of circuit operation. If the above circuits
are circuit-integrated, and the design center of an
operation speed is set at low, small size circuit
elements can be used in the IC. From this, reduction
25 in both the size of the IC chip and the cost of IC
manufacturing can be achieved.

Claims:

1. A data delay/memory circuit comprising:
(Fig. 1)
    a data shift circuit formed of a plurality of
clock-controlled data latch circuits (I1-I7) which are
cascade-connected; and
    means (CG) for supplying said plural data latch
circuits (I1-I7) with clock signals (ϕ1-ϕ7) having
individual clocking phases and being sequentially
generated such that the clocking phase (ϕ1) for a final
stage (I7) of said data latch circuits is ahead of that
(ϕ7) for an initial stage (I1) of said data latch
circuits.

2. A data delay/memory circuit according to
claim 1, characterized in that each of said data latch
circuits is of a dynamic type.

3. A data delay/memory circuit according to
claim 2, characterized in that said dynamic data latch
circuits include clocked inverters.

4. A data delay/memory circuit according to
claim 1, characterized in that said supplying means (CG)
is provided with wirings (W10-W23) for feeding said
clock signals (ϕ1-ϕ7) which geometrically cross the data
transfer direction of said cascade-connected plural data
latch circuits.

5. A data delay/memory circuit comprising:
(Figs. 3, 5)
    a plurality of data delay/memory circuits
(DMC1-DMC6) each being formed of a plurality of clock-
controlled and cascade-connected data latch circuits
(I1A-I7F):
    means (CG) for supplying said plural data latch
circuits (I1A-I7F) with clock signals (ϕ1-ϕ7) having
individual clocking phases and being sequentially
generated such that the clocking phase (ϕ1) for a final
stage (I7) of each of said data latch circuits is ahead

of that ($7) for an initial stage (I1) of each of said
data latch circuits;

serial/parallel converter means (SPC), coupled to
said data delay/memory circuits (DMC1-DMC6) and
responsive to serial input data (DX), for supplying
respective input terminals of said data latch circuits
(I1A-I1F) with data (Din1-Din6) having individual phases
with respect to said serial input data (DX); and

parallel/serial converter means (PSC), coupled to
said data delay/memory circuits (DMC1-DMC6), for
converting data (Dout1-Dout6) delivered from the
respective output terminals of said data latch circuits
(I1A-I1F) into serial output data (DY).

6. A data delay/memory circuit according to
claim 5, characterized in that each of said serial/
parallel converter means (SPC) and said parallel/serial
converter means (PSC) is controlled by a master clock
signal and formed of a plurality of cascade-connected
data delay circuits (DL10-DL20, DL22-DL32).

7. A data delay/memory circuit according to
claim 5, characterized in that each delay time of the
respective signals in said plural data delay/memory
circuits (DMC1-DMC6), which are associated with said
serial/parallel converter means (SPC) and said
parallel/serial converter means (PSC), is set at a
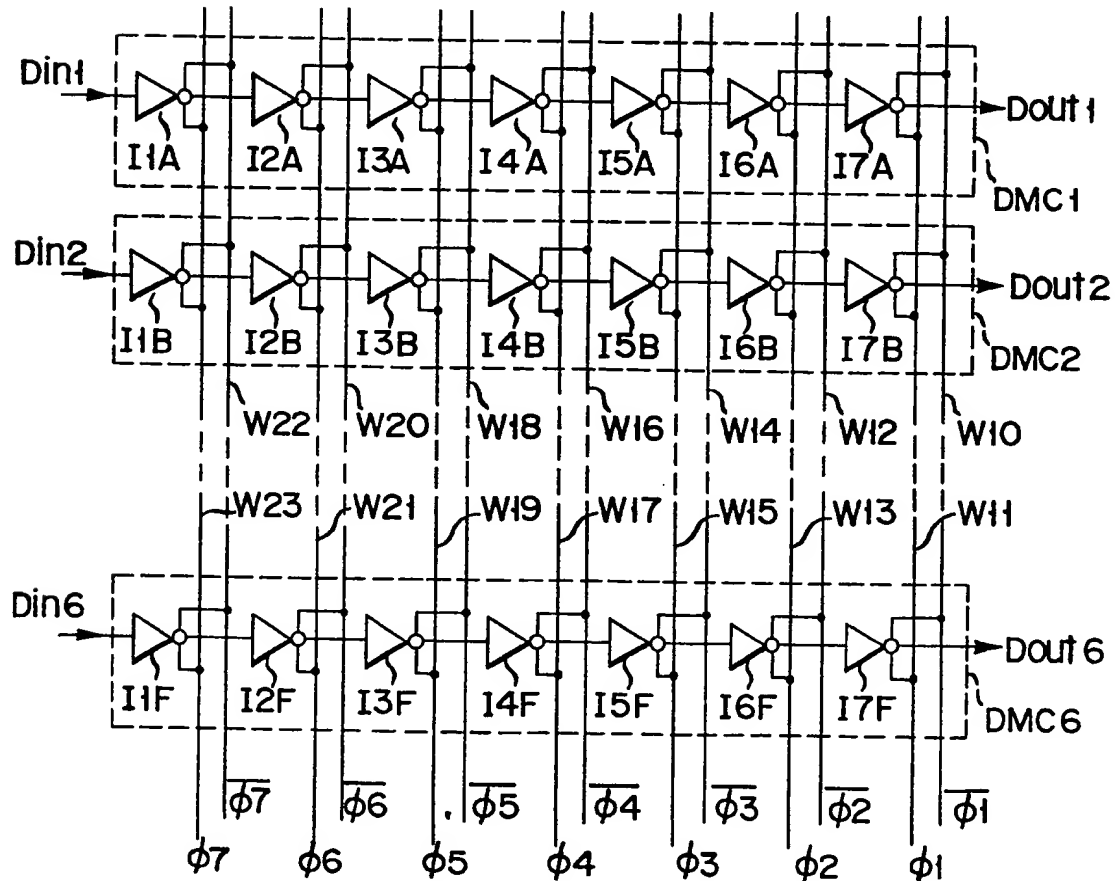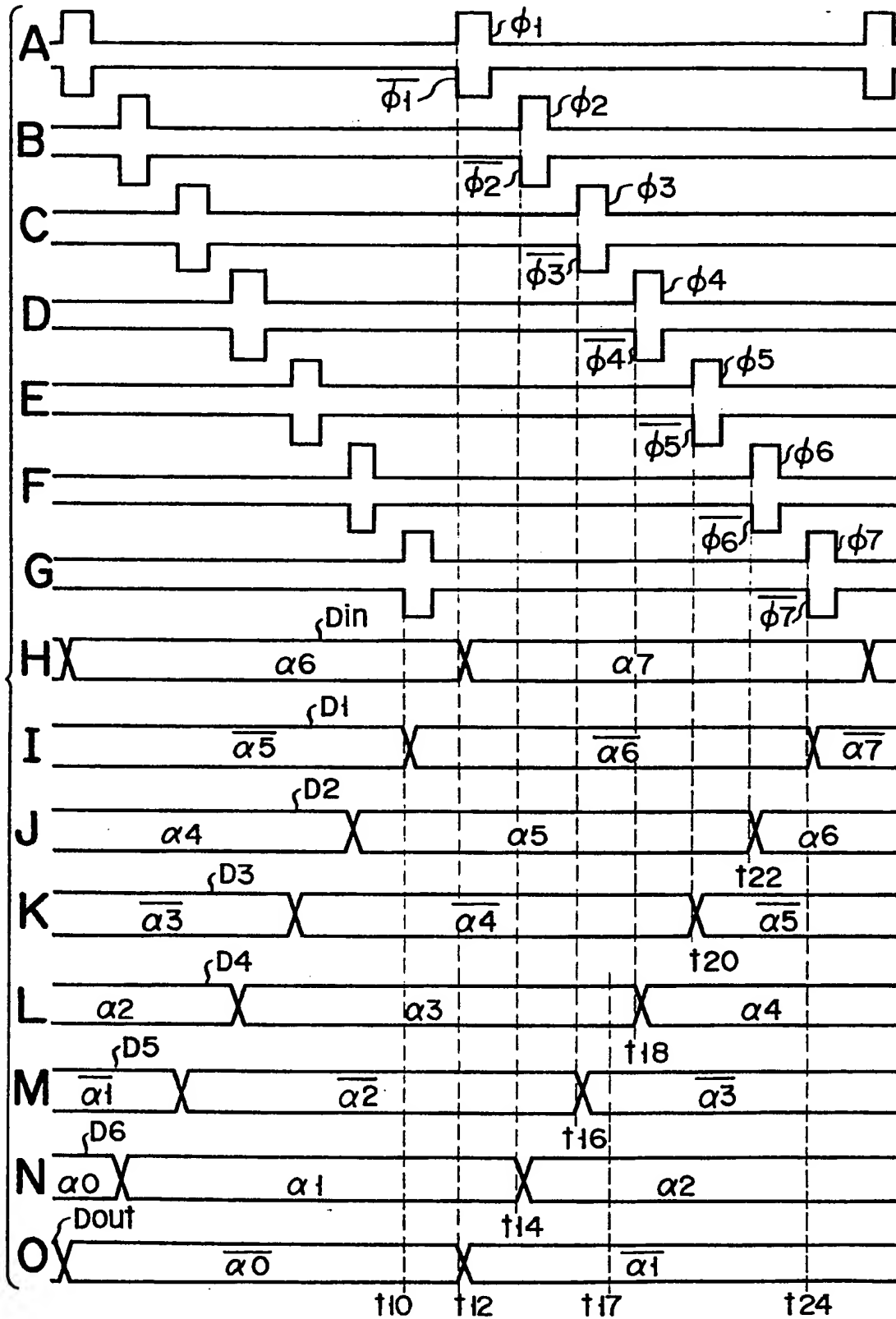prescribed value.

F I G. 1

F I G. 5

F I G. 2

F I G. 3

F I G. 4

A ϕ_{S1}

B ϕ_{S2}

C ϕ_1

D ϕ_2

E ϕ_3

F ϕ_4

G ϕ_5

H ϕ_6

I ϕ_7

J   Din1 41 35 29 23 17 11 5 41 35 29 23 17 11 5 41

K   Din2 40 34 28 22 16 10 4 40 34 28 22 16 10 4 40

L   Din3 39 33 27 21 15 9 3 39 33 27 21 15 9 3 39

M   Din4 38 32 26 20 14 8 2 38 32 26 20 14 8 2 38

N   Din5 37 31 25 19 13 7 1 37 31 25 19 13 7 1 37

O   Din6 36 30 24 18 12 6 0 36 30 24 18 12 6 0 36

P   Dout1 11 5

Q   Dout2 10 4

R   Dout3 9 3

S   Dout4 8 2

T   Dout5 7 1

U   Dout6 6 0

V   DY 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

t40
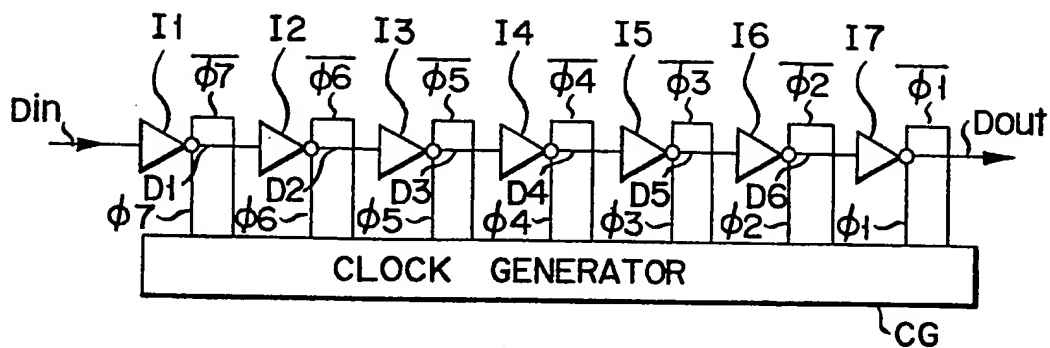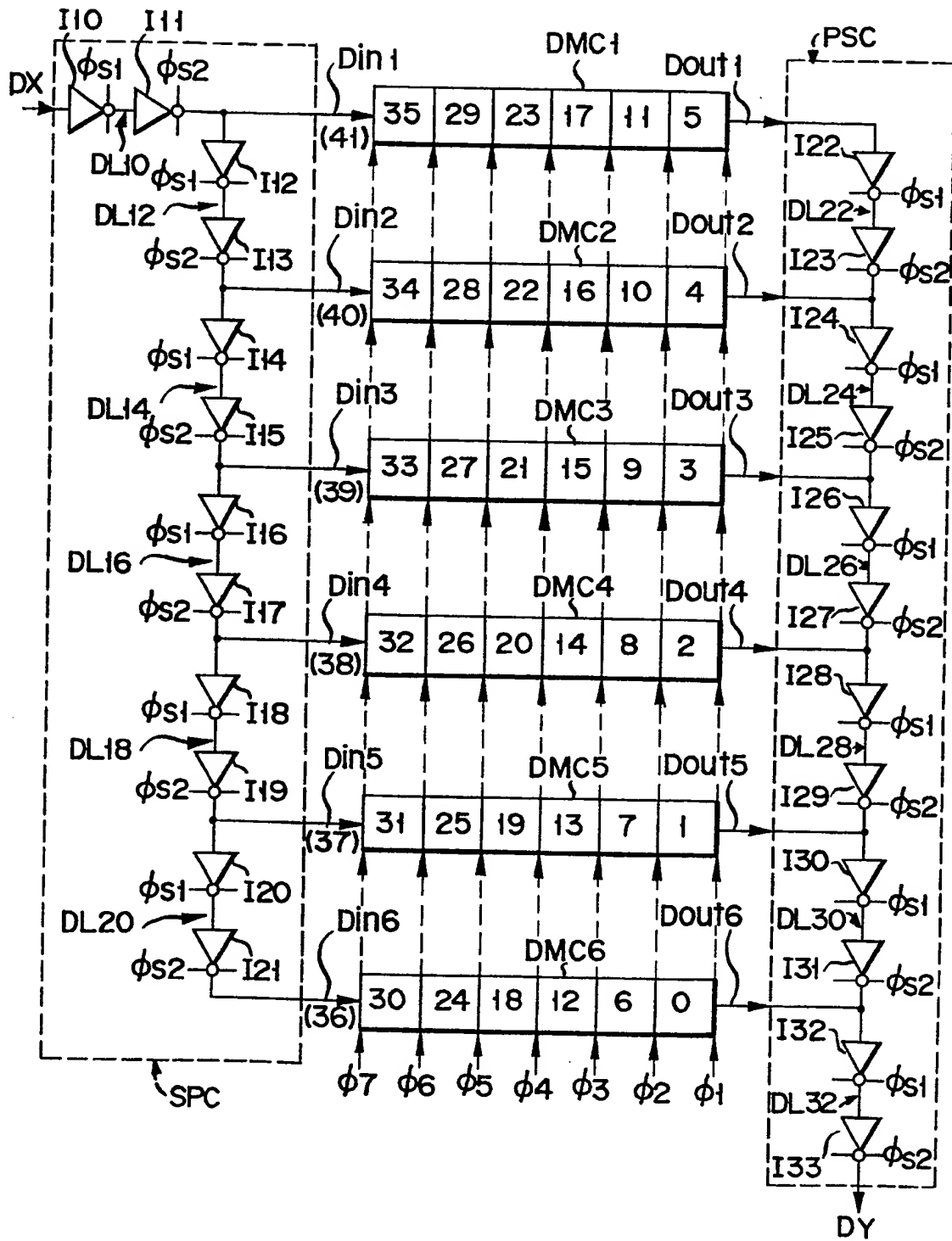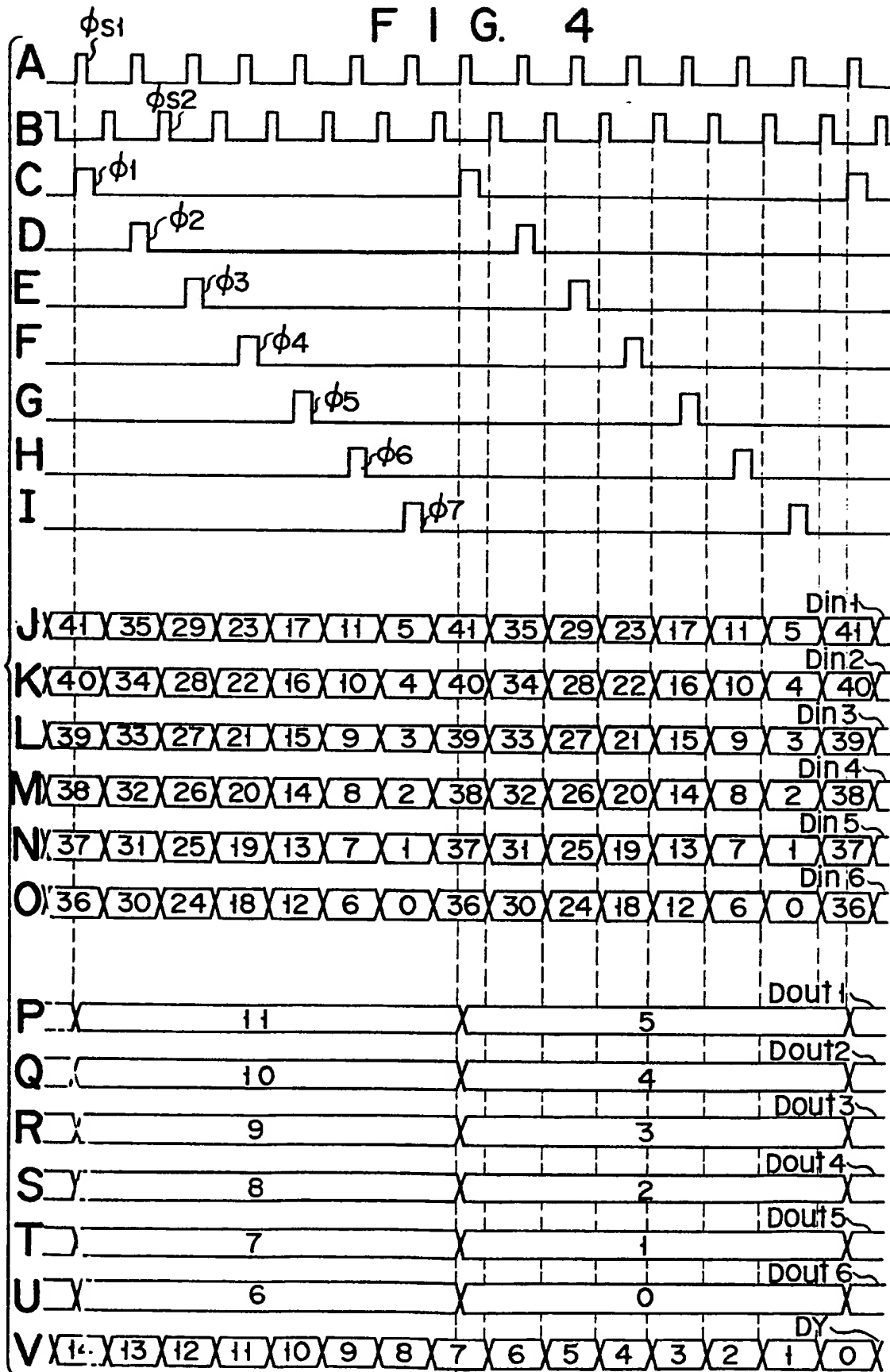
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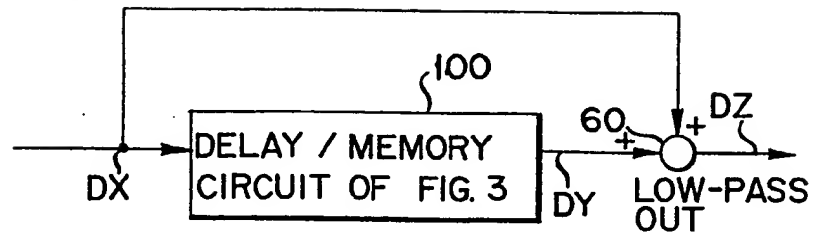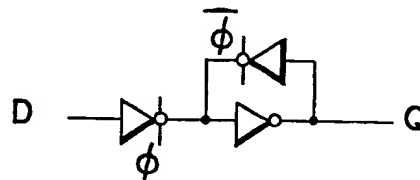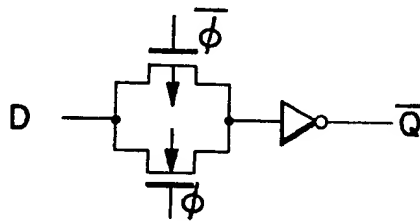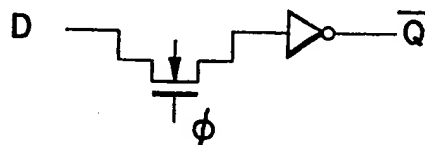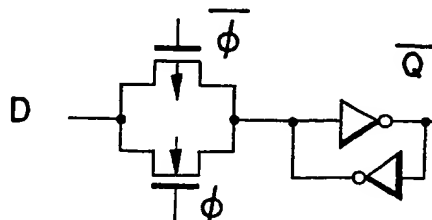

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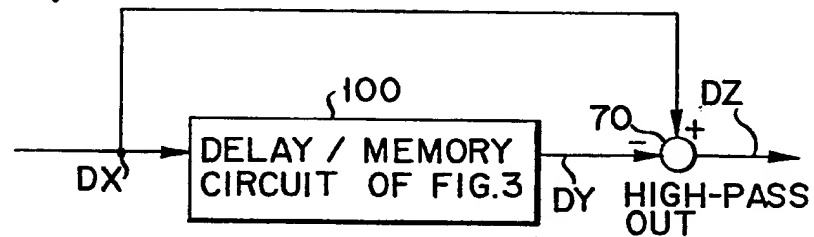
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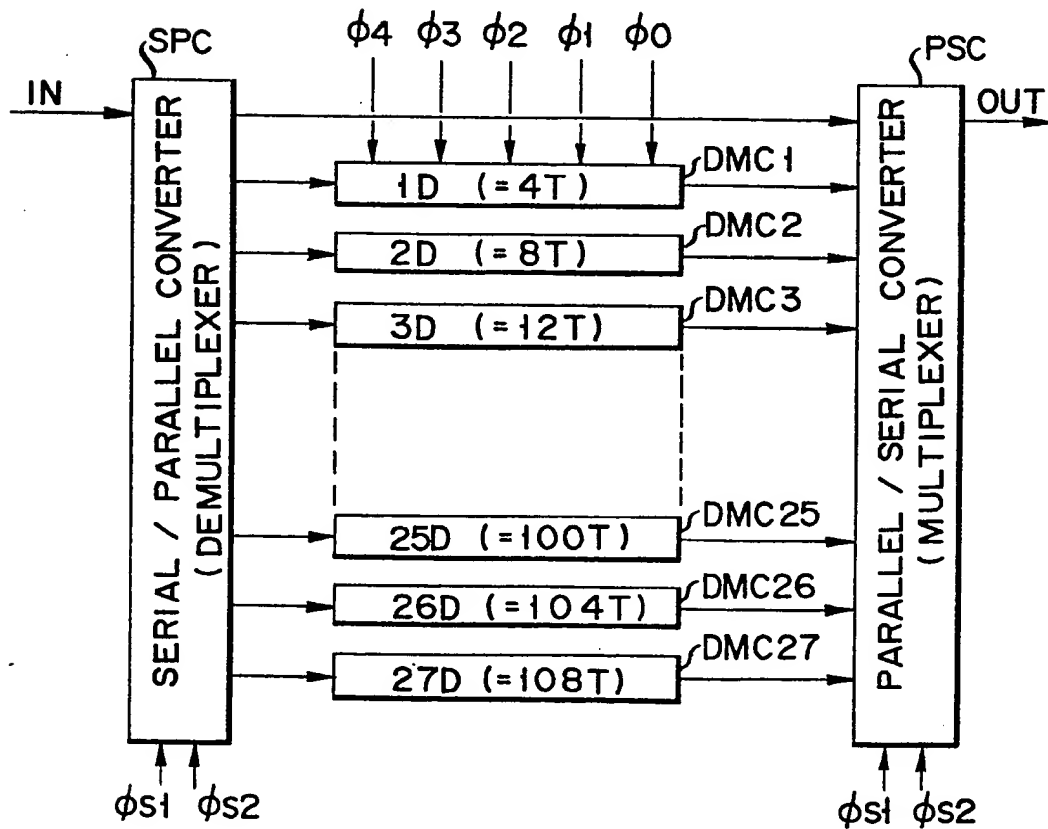
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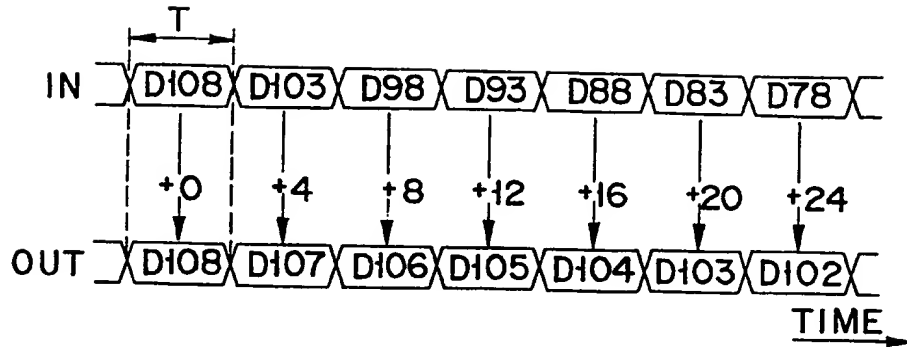
F I G. 10A

F I G. 10B

F I G. 10C

F I G. 10D

F I G. 10E